

DSPIC-BASED IMPEDANCE MEASURING INSTRUMENT

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Abstract

An implemented impedance measuring instrument is described in this paper. The device uses a dsPIC (Digital Signal Peripheral Interface Controller) as a processing unit, and a DDS (Direct Digital Synthesizer) to stimulate the measurement circuit composed by the reference impedance and the unknown impedance. The voltages across the impedances are amplified by programmable gain instrumentation amplifiers and then digitized by analog to digital converters. The impedance is measured by applying a seven-parameter sine-fitting algorithm to estimate the sine signal parameters. The dsPIC communicates through RS-232 or USB with a computer, where the measurement results can be analyzed. The device also has an LCD to display the measurement results.

Keywords: impedance measurement, dsPIC, ADC, sine-fitting.

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1. Introduction

Impedance measurement systems are used to test electronic components, circuits and materials. They can also be used to measure sensor's outputs that translate physical quantities into electrical impedance [1].

The technological advances of the past few years have improved the performance of data acquisition systems making it possible to implement cheaper ways to make the same measurements as dedicated equipment, without relevant degradation of the system accuracy.

The continuous improvement in performance of new devices such as analog to digital converters (ADCs), combined with more powerful signal processing techniques, are some of the factors that have contributed to this trend.

Typically, impedance measurement systems operate in a reduced frequency range or have a very high price. The 4294A Precision Impedance Analyzer from Agilent Technologies [2], one of the leading companies that sell impedance measurement systems, performs measurements from 40 Hz up to 110 MHz with a basic accuracy of 0.08 % and costs around 30.000 €, which makes it understandable why many companies and research institutes may have some difficulties acquiring such an expensive device.

To cope with this issue, it is important to pursue alternative solutions to make impedance measurements with a comparable accuracy to that of sophisticated commercially available impedance measurement systems.

The instrument developed in this work strives to achieve this objective. It is based on a dsPIC (Digital Signal Peripheral Interface Controller), which is responsible for controlling all the hardware and performing the necessary signal processing. The most important signal processing techniques used are the sine-fitting algorithms, which allow the estimation of the impedance under measurement.

Sine-fitting algorithms are used to estimate a set of parameters that best fit a given sine signal. The existing sine-fitting algorithms encompass the three and four-parameter

sine-fitting algorithms, which were standardized in [3], and the seven-parameter sine-fitting algorithm [4]. The algorithms are similar in nature, but the three-parameter algorithm is non-iterative while the four- and seven-parameter algorithms are iterative. The seven-parameter algorithm differs from the four-parameter algorithm in the sense that it uses the data from two acquisition channels with a common frequency to obtain a better resolution of the estimated sine signals parameters.

The implemented instrument in this work has certain similarities to that of [5], but instead of a function generator to stimulate the measurement circuit it uses a DDS (Direct Digital Synthesizer), and rather than using a DSP (Digital Signal Processor) it uses a dsPIC as the processing unit. The instrument is capable of measuring impedances ranging from 10 mΩ to 10 kΩ at frequencies between 200 Hz and 200 kHz.

2. Implemented Architecture

2.1. Measurement Circuit and Method

The measurement method used to determine the impedance under measurement is based in the volt-ampere method [6]. The amplitude of the unknown impedance can be calculated based on the values of the amplitude of the reference impedance and the amplitudes of the sine signals across each impedance. The phase is obtained using the phase of the reference impedance and the phase difference between the sine signals across the impedances.

The circuit used for the measurement of the unknown impedance is represented in Fig. 1.

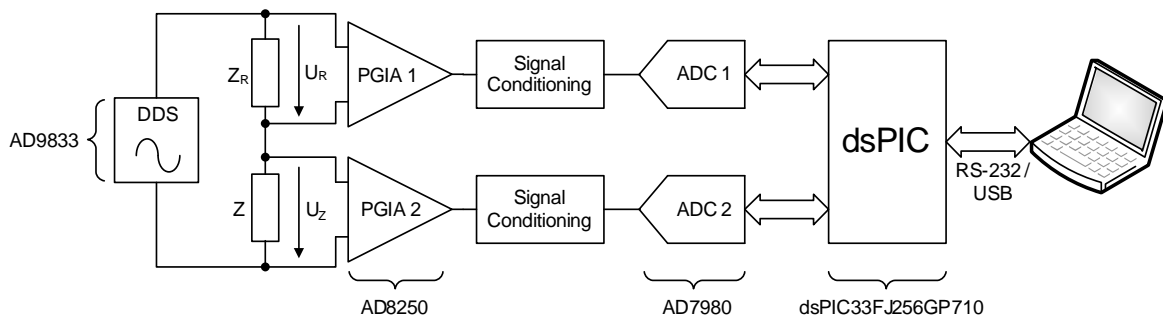


Fig. 1. Measurement circuit. Z is the impedance to be measured and Z_R is the reference impedance.

The implemented instrument has the ability to select different reference impedances according to the amplitude of the impedance under measurement in order to maximize the use of the ADCs dynamic range. For this purpose, six relays are used to choose the reference impedance among a fixed set of six resistors. The resistors have a $\pm 5\%$ tolerance and their nominal values are 100 Ω, 200 Ω, 500 Ω, 1000 Ω, 2000 Ω and 5000 Ω. They were characterized using the 3532-50 LCR HiTESTER from HIOKI [7], which determines the values of the reference impedances with 0.08 % accuracy

The relays used are the A5W-K from Takamisawa and they are connected according to the setup presented in Fig. 2. Using this setup we can avoid measuring the impedance of the relays itself, thus minimizing the errors associated with the impedance measurement.

With the lowest reference resistor of 100 Ω, 10 mΩ was the minimum impedance amplitude that the system could measure, because of the low signal amplitude across the impedance under measurement. The maximum impedance amplitude possible to measure is 10 kΩ due to the values of the reference impedances available. Nevertheless, a larger measurement range can be obtained if the reference impedance values are changed to cover a wider range.

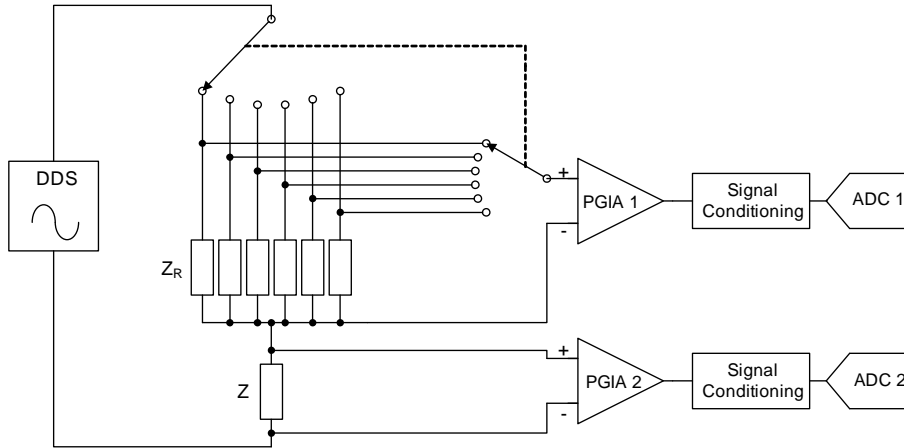


Fig. 2. Setup used for the relays to select different reference impedances.

The signal conditioning blocks represented in Fig. 1 and Fig. 2 are composed by a differential amplifier circuit used to add a DC offset to the signals to be acquired. This circuit is necessary because the ADCs used in the instrument can only acquire positive signals and the signals across the impedances are bipolar.

The input structure of the used ADCs incorporates a low-pass filter which reduces undesirable aliasing effects.

The instrument follows the following procedure to determine the unknown impedance:

1. The dsPIC controls the DDS to generate a sine signal with the user-defined measurement frequency using the SPI (Serial Peripheral Interface) protocol.
2. The gains of the PGIAs (Programmable Gain Instrumentation Amplifiers) are set and the reference impedance is chosen. This is done according to the amplitude of the unknown impedance and the amplitude of the sine signals across each impedance.
3. The ADCs acquire simultaneously 1024 samples per channel. The sampling rate used is selected based on the measurement frequency. The dsPIC communicates with the ADCs also with the SPI protocol.
4. The dsPIC processes the acquired samples and applies the three- and seven-parameter sine-fitting algorithms to determine the amplitude ($|Z|$) of the unknown impedance using

$$|Z| = |Z_R| \times \frac{|U_Z|}{|U_R|}, \quad (1)$$

and its phase (ϕ_Z) using

$$\phi_Z = \phi_{Z_R} + (\phi_{U_Z} - \phi_{U_R}). \quad (2)$$

$|Z_R|$ and ϕ_{Z_R} are the amplitude and phase of the reference impedance at the measurement frequency, $|U_Z|$ and ϕ_{U_Z} represent the amplitude and phase of the signal across the unknown impedance, while $|U_R|$ and ϕ_{U_R} are the amplitude and phase of the signal across the reference impedance.

5. The measurement results are displayed in the LCD and can be sent to a PC (Personal Computer) using a RS-232 or USB connection, where the user can interpret and save them.

2.2. Description of the hardware

Table 1 describes the devices used in the implemented impedance measuring instrument.

Table 1. Description of the devices used in the instrument.

Devices	Description
ADCs	Successive approximation ADC; 16 bit resolution; 1 MS/s maximum conversion speed; SPI compatible.
DDS	Capable of generating sine, triangle and square waveforms; 28 bit resolution; THD (Total Harmonic Distortion) of 51 dB for a sine signal; SPI compatible.
dsPIC	40 MIPS maximum throughput; 256 kB flash program memory; 30 kB RAM.
PGIAs	4 digitally controlled programmable gains: 1, 2, 5 and 10.
Relays	2 poles; nominal voltage of 5 V.

Although the ADCs have a maximum conversion speed of 1 MS/s, it was not possible to use the full capabilities of the ADCs due to limitations introduced by the SPI module of the dsPIC used to control them. To read the samples of both ADCs (32 bits) and use a conversion speed of 1 MS/s an SPI module operating at 32 MHz was necessary. However, the SPI module only operates at a maximum frequency of 10 MHz, which limited the maximum conversion speed of the ADCs to 178 kS/s.

3. Algorithms

3.1. Sampling Frequency

As stated before, the implemented instrument has the ability to measure impedances up to 200 kHz. Because the maximum usable sampling frequency of the ADCs is 178 kS/s (F_{Smax}), it was necessary to take into account two situations when acquiring the signals: the situation of undersampling and the situation of no undersampling. In the case of no undersampling the sampling frequency is chosen in a way that guarantees that at least eight periods of the signals are acquired. In the case of undersampling, the sampling frequency is set considering

$$m_{real} = \left\lfloor \frac{f}{F_{Smax}/2} \right\rfloor, \quad (3)$$

$$m_{ideal} = m_{real} + 0.5, \quad (4)$$

and

$$F_S = \frac{2 \times f}{m_{ideal}}, \quad (5)$$

where f is the measurement frequency, m_{real} is the full number of folds of the frequency spectrum, m_{ideal} is the desired number of folds of the frequency spectrum so that the acquired signal's apparent frequency will be in the middle of the frequency spectrum (which is the best case) and F_S is the selected sampling frequency.

It is possible to determine the number of folds of the signal spectrum because the measurement frequency is known in advance, since it is set by the user.

3.2. Three-Parameter Sine-Fitting

The three-parameter sine-fitting algorithm is non-iterative and with prior knowledge of the signal frequency, it is capable of estimating the amplitude, phase and DC component of a given sine signal [3].

The acquired sine signals can be modeled by

$$u(t) = D \cos(2\pi ft + \phi) + C, \quad (6)$$

or

$$u(t) = A \cos(2\pi ft) + B \sin(2\pi ft) + C, \quad (7)$$

considering

$$D = \sqrt{A^2 + B^2}, \quad (8)$$

and

$$\phi = -\text{atan2}(B, A), \quad (9)$$

where D and ϕ are the amplitude and phase of the sine signal, and C its DC component. A and B are the in-phase amplitude and the in-quadrature amplitudes of the sine signal, respectively.

The parameter vector estimated by the algorithm is

$$\hat{\mathbf{x}} = [A \quad B \quad C]^T = \mathbf{M}^\dagger \mathbf{y}, \quad (10)$$

where \mathbf{y} is the acquired samples vector

$$\mathbf{y} = [u_1 \quad u_2 \quad \dots \quad u_N]^T, \quad (11)$$

and the matrix \mathbf{M} is defined by

$$\mathbf{M} = \begin{bmatrix} \cos(2\pi ft_1) & \sin(2\pi ft_1) & 1 \\ \vdots & \vdots & \vdots \\ \cos(2\pi ft_N) & \sin(2\pi ft_N) & 1 \end{bmatrix}. \quad (12)$$

N is the number of acquired samples per channel. \mathbf{M}^\dagger is the pseudo-inverse matrix of \mathbf{M} .

The frequency used in the three-parameter algorithm is estimated using both the FFT (Fast Fourier Transform) and IpDFT (Interpolated Discrete Fourier Transform) algorithms [8].

3.3. Seven-Parameter Sine-Fitting

Unlike the three-parameter sine-fitting algorithm, the seven-parameter algorithm is iterative and it estimates the common signal frequency of both acquisition channels, along with the amplitudes, phases and DC components of each channel [4].

To ensure that the algorithm converges, it is imperative to provide the best possible initial estimates to the algorithm. For this reason, the three-parameter and IpDFT algorithms are used. Convergence is achieved when the absolute relative frequency adjustment, $|\Delta f^{(i)} / f^{(i)}|$, is below the preset threshold of 5×10^{-7} . $\Delta f^{(i)}$ is the frequency correction that updates the estimated common frequency in each iteration of the algorithm.

When the algorithm converges, it is then possible to obtain an estimate for the amplitude and phase of the impedance under measurement using (1) and (2) respectively.

Instead of using the seven-parameter sine-fitting algorithm, it is possible to use the four-parameter sine-fitting algorithm and apply it to the samples of each acquisition channel individually. However, in [9], it was shown that the seven-parameter algorithm is more effective when compared to the application of two four-parameter algorithms.

The output frequency of the DDS is expressed as a fraction of a master clock which is provided by a DDS external oscillator. The accuracy of the output frequency of the DDS will depend on this oscillator whose frequency is not accurately known. So, the frequency programmed for the measurement may differ from the frequency that is actually generated by the DDS. Also, the sampling rate of the ADCs, which is controlled by the dsPIC, has an inherent uncertainty associated with it. This may affect the convergence time of the seven-parameter sine-fitting algorithm when estimating the signal frequency since these algorithms actually estimate the ratio between the signal frequency and the sampling rate. By estimating the signal frequency with the IpDFT algorithm it is possible to obtain a very close estimate of the real frequency of the signal that is being applied to the measurement circuit. With a good-enough initial estimate of the signal frequency, the iterations of the seven-parameter sine-fitting algorithm are reduced, which reduces the computational time of the measurement.

4. Compensation Techniques

Sophisticated impedance measurement systems employ advanced compensation techniques in order to improve the accuracy of the measurements. These techniques aim to account for any residual parasitic components present at the test fixtures or test cables used to measure the impedance, thus minimizing the errors associated with the impedance measurement.

The most widely applied compensation techniques in impedance measurements are the OPEN, SHORT and LOAD compensations [6], although some systems only make use of the OPEN and SHORT compensations [7].

For the purposes of this work only the OPEN and SHORT compensations were considered. This compensation technique assumes that the residuals of the test fixtures or test cables can be modeled using an L/R/C/G circuit, as represented in Fig. 3.

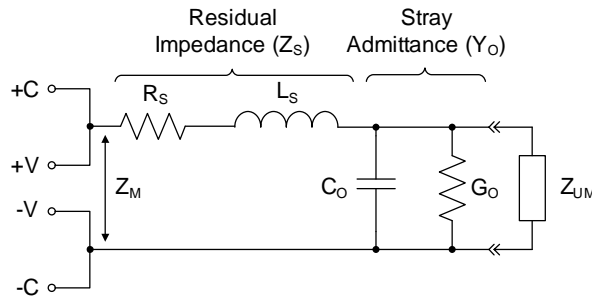


Fig. 3. Test fixture / Test cables residuals. Z_{UM} is the impedance under measurement and Z_M is the impedance that is actually measured.

As presented in Fig. 3 the measurement is done using a four-terminal configuration, where +C and -C represent the current connections and +V and -V the voltage connections to the impedance. Z_{UM} is the impedance under measurement, while the impedance that is actually measured is represented by Z_M .

To measure the stray admittance Y_o , represented by

$$Y_o = G_o + j\omega C_o, \quad (13)$$

the terminals connected to the impedance under measurement are left open as shown in Fig. 4(a). This way the value of the residual impedance Z_s is negligible.

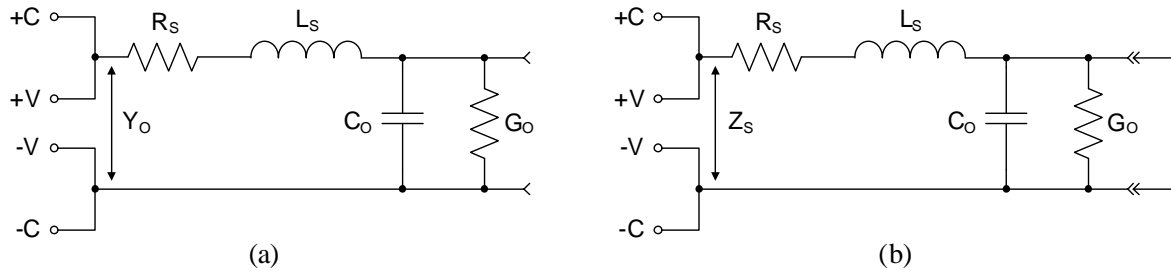


Fig. 4. (a) Measurement circuit for OPEN compensation. (b) Measurement circuit for SHORT compensation.

To determine the residual impedance Z_S , represented by

$$Z_S = R_S + j\omega L_S, \quad (14)$$

the stray admittance is bypassed by shortening the terminals connected to the impedance under measurement as shown in Fig. 4(b).

After the OPEN and SHORT compensation procedures are finished and all the residual parameters are determined, we can use the values of Y_O and Z_S to correctly determine the impedance under measurement based on the impedance measured value (Z_M) by using

$$Z_{UM} = \frac{Z_M - Z_S}{1 - (Z_M - Z_S) \times Y_O}. \quad (15)$$

The OPEN and SHORT compensations are done by performing a frequency sweep in the measurement frequencies range. A frequency sweep between 200 Hz and 200 kHz with one thousand points was done. The impedance amplitude and phase were recorded and then used to correct the measurements done from that point on. If the measurement set-up (measurement cables) changes, it is necessary to repeat the OPEN and SHORT compensations to correctly compensate the new set-up.

The imperfections of the measurement channels were also taken into account by performing a calibration procedure. The same signal was applied to both acquisition channels (which includes the PGIA, the signal conditioning circuit and the ADC) and the amplitude of each channel and the phase difference between them were measured and stored, and then used to correct the measurements. During the measurements, the gains of the PGIAs are not necessarily the same, so this procedure was done for all combinations of the PGIA gains.

The mismatch of both ADCs (magnitude and phase) is also taken into account, given that this procedure is done by applying the signal to the entire acquisition channel.

5. Control Software

A software application, running on a PC, which is used to control the developed instrument, was implemented. The program acts as an interface between the user and the device enabling him to select the measurement frequency and monitor the device. The user can view the acquired samples of the signals across the impedances and can choose whether he wants to save the measurement results or not. The acquired samples are only transferred to the PC if the user requests them. This software application is useful but also necessary because the device is not a standalone instrument. The control software was developed in the LabVIEW environment, which offers simple and intuitive programming tools, thus facilitating the implementation of the software application for the impedance measurement instrument.

6. Experimental Results

Two impedances were tested with a frequency sweep of two hundred points performed between 200 Hz and 200 kHz. The results were compared with a commercially available impedance measurement system, the 3532-50 LCR HiTESTER from HIOKI, and with the results obtained when no compensation techniques are used in the implemented instrument. One of the impedances was composed by a 36 Ω resistor in series with a 2 mH inductance, while the other by a 2 k Ω resistor in series with a 180 nF capacitor.

Fig. 5 shows the amplitude and phase of the first impedance. Fig. 7 represents the amplitude and phase of the second one. Fig. 6 and Fig. 8 show the relative measurement errors of the first and second impedance, respectively, using as a reference the measurement results obtained with HIOKI, for both the compensated and not compensated instrument. Z_m represents the complex value of the measured impedance with the instrument and Z_H the equivalent measured results with HIOKI.

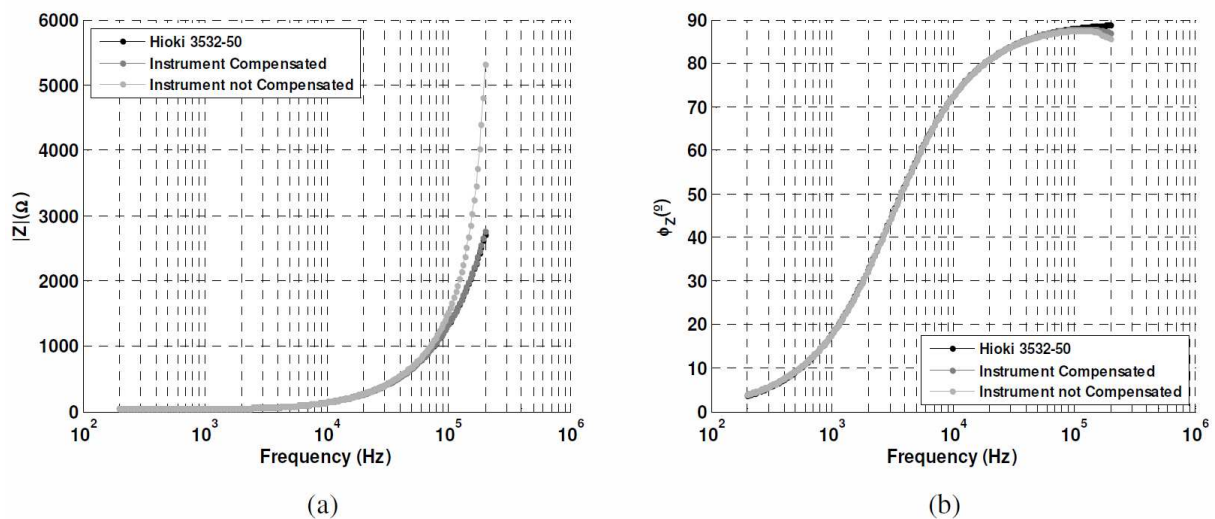


Fig. 5. Amplitude (a) and phase (b) of an impedance, composed by a 36 Ω resistor in series with a 2 mH inductance.

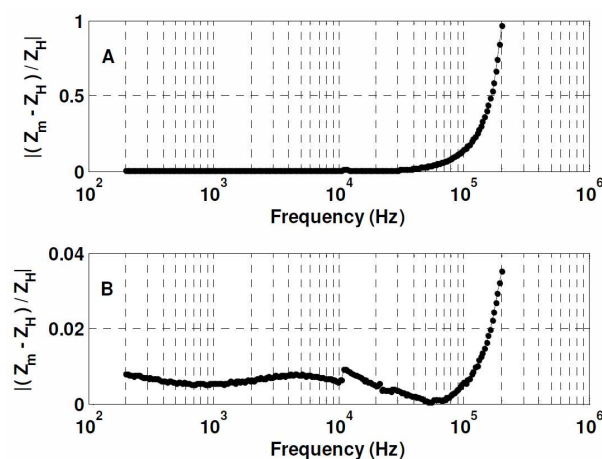


Fig. 6. Relative measurement errors for the impedance composed by a 36 Ω resistor in series with a 2 mH inductance using HIOKI's measurements as a reference. A is for the not compensated instrument and B for the compensated.

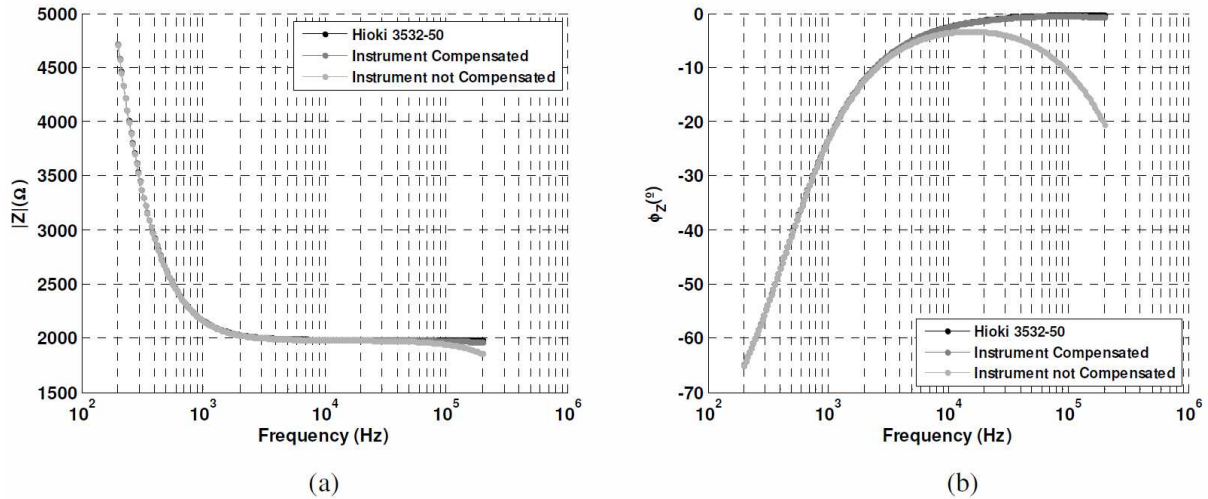


Fig. 7. Amplitude (a) and phase (b) of an impedance, composed by a 2 k Ω resistor in series with a 180 nF capacitor.

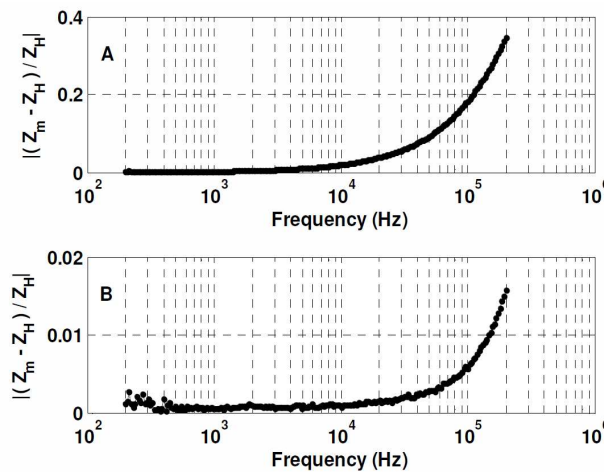


Fig. 8. Relative measurement errors for the impedance composed by a 2 k Ω resistor in series with a 180 nF capacitor using HIOKI's measurements as a reference. A is for the not compensated instrument and B for the compensated.

The results presented in Fig. 5, 6, 7 and 8 prove that it is of utmost importance to compensate for the residuals introduced by the test fixture or test cables connected to the impedance under measurement. The influence of such residuals becomes more relevant as the measurement frequency increases, as demonstrated by the presented results.

Table 2 presents the measurement results obtained at 1 kHz for three resistors of 10 m Ω , 100 m Ω and 10 k Ω , a 180 nF capacitor and a 15 mH inductance.

Table 2. Measurement results obtained with the Hioki 3532-50 and the implemented instrument at 1 kHz.

Impedance		R = 10 m Ω	R = 100 m Ω	L = 15 mH	C = 180 nF	R = 10 k Ω
Hioki 3532-50	$ Z $ (Ω)	10.03 m	99.22 m	106.09	858.38	9897.50
	ϕ ($^\circ$)	-0.22	0.42	69.44	-89.72	0.00
Instrument Compensated	$ Z $ (Ω)	9.98 m	99.30 m	104.86	857.11	9895.48
	ϕ ($^\circ$)	-1.56	0.072	69.16	-89.73	-0.00014
Instrument not Compensated	$ Z $ (Ω)	15.23 m	101.22 m	104.88	856.09	9892.87
	ϕ ($^\circ$)	39.19	5.81	69.47	-89.73	-0.58

The results presented in Table 2 support what was already demonstrated in Fig. 5 to 8, *i.e.*, the importance of compensating the influence of the residuals introduced by the test fixture or test cables used to measure an impedance. In Table 2 it is possible to see that the compensation is more relevant for the lowest value resistors, particularly for the phase measurement, although the amplitude is also affected.

Ten thousand measurements of a resistor with a nominal value of 1.8 k Ω were taken at 1 kHz and 200 kHz. A capacitor of 32 nF was also measured at 1 kHz. The histograms of the amplitude and phase of the impedances were obtained and they are represented in Fig. 9, Fig. 10 and Fig. 11. μ represents the mean, σ_0 the standard deviation and σ_0/μ the relative standard deviation of the measurements.

The standard deviations for the 1.8 k Ω resistor when measured at 200 kHz (Fig. 10) are higher when compared to the measurements performed at 1 kHz (Fig. 9). Also, at 200 kHz the mean values are slightly shifted from those obtained at 1 kHz. This is due to the fact that the measurements were done at the worse measurement frequency region for the device, where the relative measurement error is higher, as shown in Fig. 6 and Fig. 8.

The measurements were done over a long period of time, around twenty hours. This long measurement time can be attributed partially to the complexity of the algorithms used and to the low throughput capabilities of the dsPIC. The execution times of the algorithms used to process the acquired samples were measured: 943 ms for the FFT, 14 ms for the IpDFT, 1.8 s for the three-parameter sine-fitting and 3.6 s for the seven-parameter sine-fitting. Typically an acquisition takes 16 ms to complete (at 1 kHz), and it takes around 33 ms to transfer the acquired samples and the measurement results to the computer (using the USB connection). Two acquisitions and two executions of the three-parameter sine-fitting algorithm are necessary: one for the estimation of the gains of the PGIAs and the reference impedance to use, and another for the final measurement.

All algorithms are executed in the dsPIC. The acquired samples are only transferred to the PC if the user requests them in the control software application running on the PC, and in this case the samples are only used to represent the acquired signals across each impedance.

The standard deviations of the performed measurements are very low. During the long measurement cycle, a 3 °C ambient temperature variation was observed, which leads us to assume that the instrument presents a stable behavior when it comes to temperature variations.

The results presented in Fig. 9, 10 and 11 demonstrate the capabilities of the developed instrument which, at a reduced cost, is still capable of producing measurements with comparable accuracy to that of expensive dedicated impedance measurement systems.

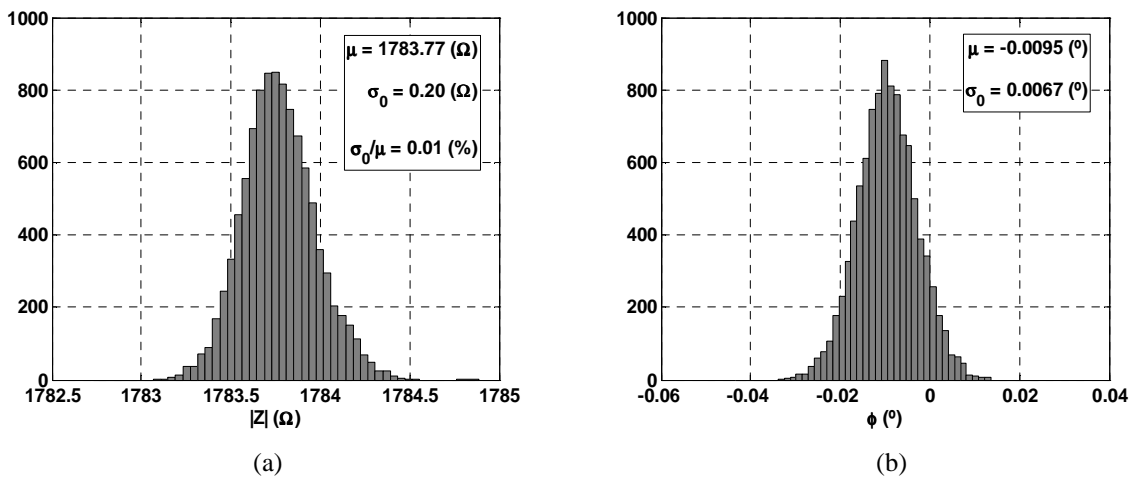


Fig. 9. Amplitude (a) and phase (b) histograms for a 1.8 k Ω resistor measured at 1 kHz.

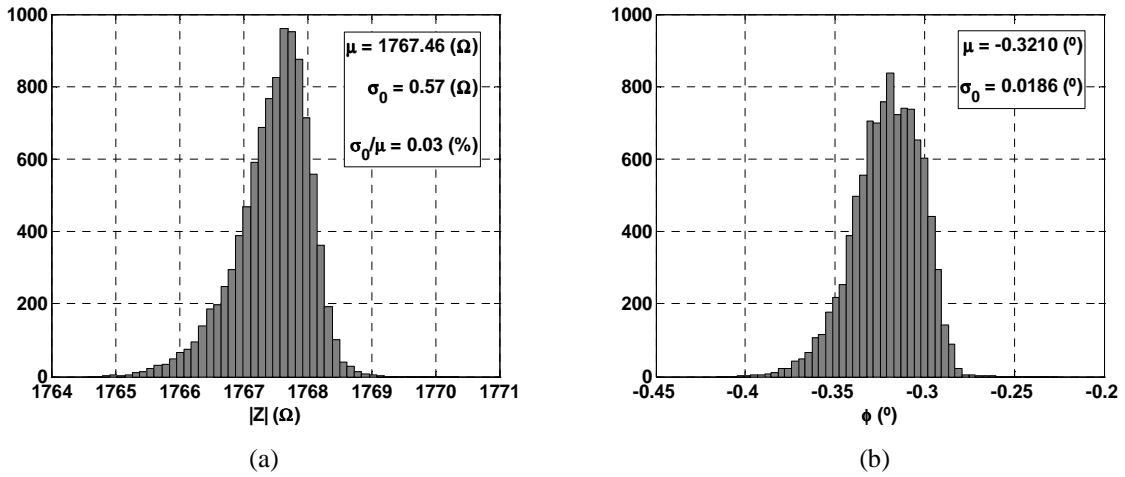


Fig. 10. Amplitude (a) and phase (b) histograms for a 1.8 k Ω resistor measured at 200 kHz.

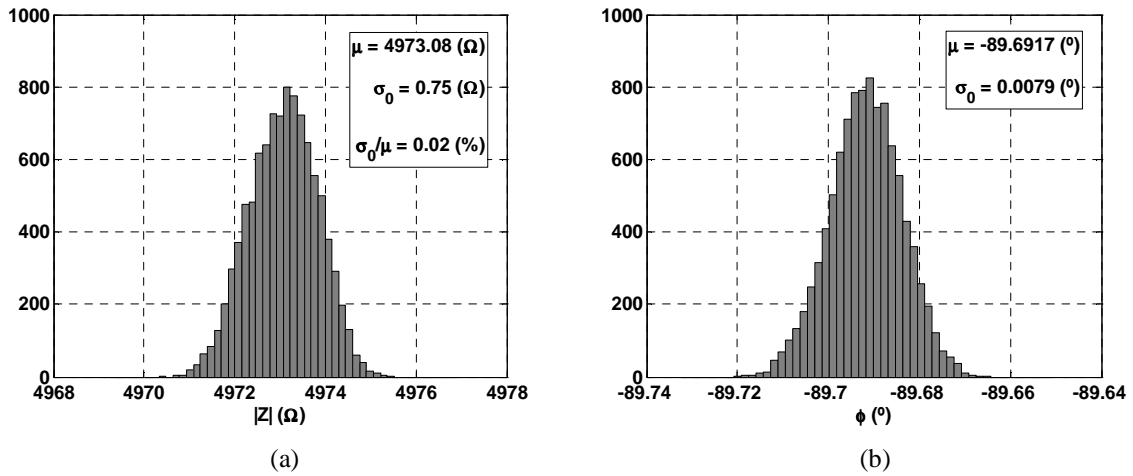


Fig. 11. Amplitude (a) and phase (b) histograms for a 32 nF capacitor measured at 1 kHz.

The uncertainty regions of the measurements with a confidence level of 68 % and 95 % along with the correspondent histograms are represented in Fig. 12, Fig. 13 and Fig. 14.

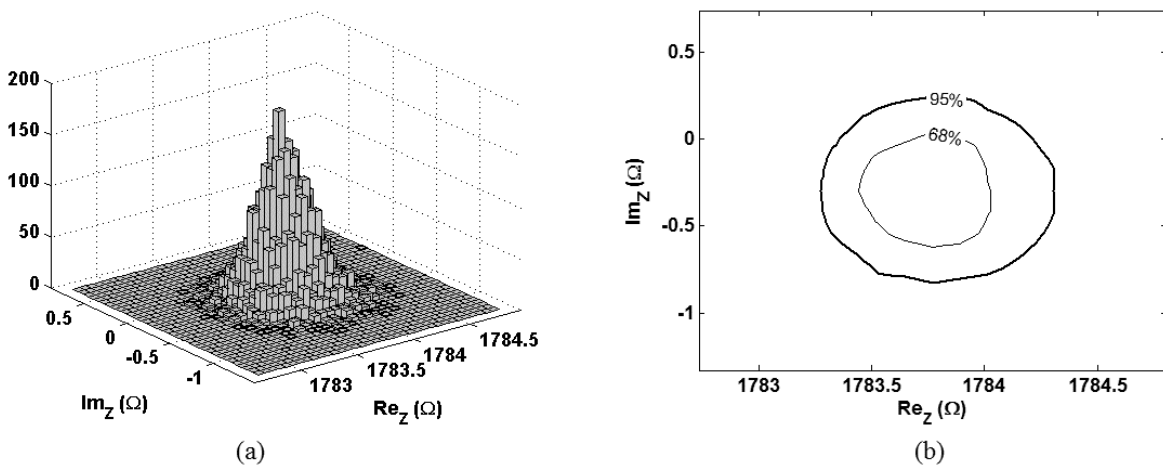


Fig. 12. Histogram (a) and correspondent uncertainty regions with 68 % and 95 % confidence levels (b) for a 1.8 k Ω resistor measured at 1 kHz.

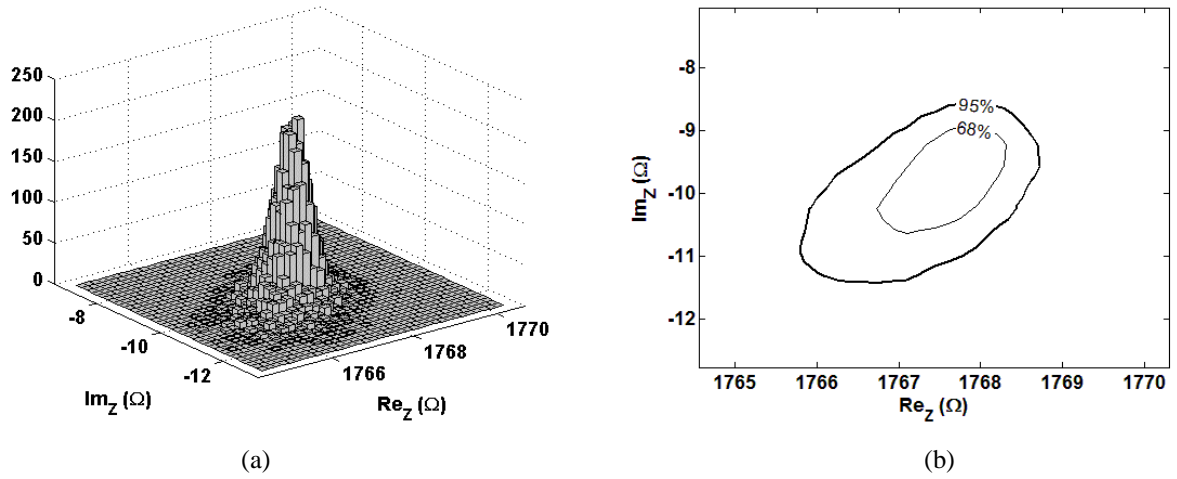


Fig. 13. Histogram (a) and correspondent uncertainty regions with 68 % and 95 % confidence levels (b) for a 1.8 k Ω resistor measured at 200 kHz.

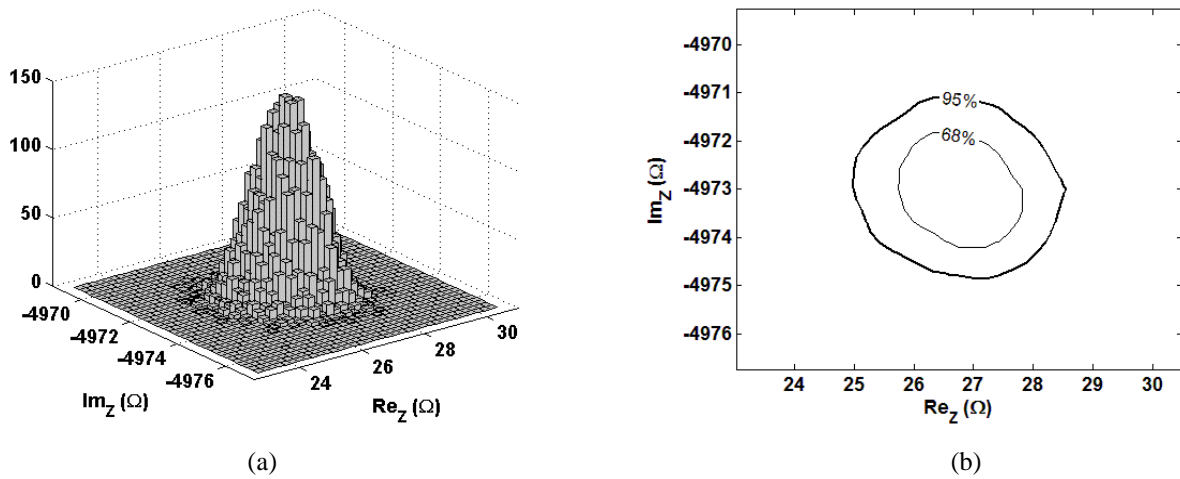


Fig. 14. Histogram (a) and correspondent uncertainty regions with 68 % and 95 % confidence levels (b) for a 32 nF capacitor measured at 1 kHz.

The implemented impedance measurement instrument is presented in Fig. 15.

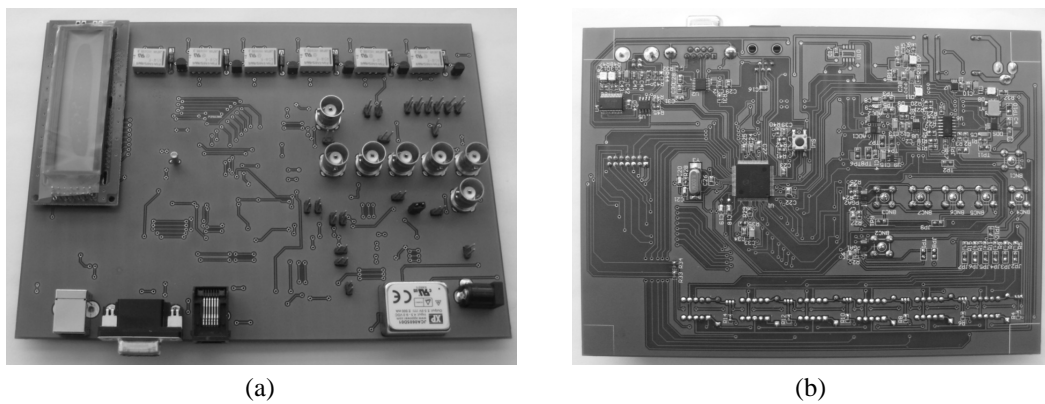


Fig. 15. Implemented instrument: (a) top view; (b) bottom view.

7. Conclusions

Given the high cost of sophisticated impedance measurement systems, it is important to implement alternative ways to make the same measurements as these systems without relevant degradation of the system accuracy. This will enable most companies and research institutes to purchase impedance measurement systems, at a reduced cost, capable of rivaling with existing commercial devices. The implemented impedance measurement instrument aims to fulfill this objective. It makes use of the processing capabilities of the processing unit used (dsPIC) associated with powerful signal processing techniques, such as the sine-fitting algorithms, to obtain comparable results to that of dedicated impedance measurement systems.

Although the processing capabilities of the selected dsPIC are quite satisfactory, it was concluded that it has a limited throughput capability for our application. This resulted in a long measurement time, mainly due to the complexity of the algorithms used to estimate the impedance under measurement like the seven-parameter sine-fitting algorithm. This is why the upgrade of the processing unit from a dsPIC to a DSP with a higher throughput and increased memory for data (to be able to process a larger number of samples) is being considered.

The developed instrument is capable of measuring impedances in the amplitude range from 10 m Ω to 10 k Ω at frequencies ranging from 200 Hz up to 200 kHz, and it makes it easy for a user to interact with the device due to its USB and RS-232 connections to a PC. Through the PC the user can select the measurement frequency, monitor the device and choose to save the measurement results. The instrument uses the OPEN and SHORT compensation techniques to account for any residuals introduced by the test fixture or test cables connected to the impedance under measurement and minimize the errors associated with the measurement of the impedance.

Several impedances were tested and the presented results were compared with the 3532-50 LCR HiTESTER from HIOKI. The results demonstrated that it is possible to implement a low cost device capable of producing results comparable with those obtained by a commercially available impedance measurement system. The results also proved the importance of using compensation techniques to reduce the errors of the impedance measurement to a minimum.

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